Claims

[c1] A method for forming a CMOS device comprising the steps of:

(a) providing a patterned gate stack on a surface of a semiconductor substrate, said patterned gate stack including gate dielectric below a gate conductor with exposed vertical sidewalls;

(b) forming a dielectric layer over said gate region, exposed vertical sidewalls and substrate surfaces;

(c) forming a spacer element overlying said dielectric layer formed at each vertical sidewall, said spacer comprising a nitride layer;

(d) removing said dielectric layer using an etch process such that a portion of said dielectric layer underlying each said spacer remains;

(e) forming a thin nitride layer over said gate region, said spacer elements, and said substrate surfaces;

(f) etching said thin nitride layer to create a nitride plug layer that encapsulates and seals at least a portion of said dielectric layer underlying each said spacer;

(g) performing a pre-silicide clean process for removing material remaining on said substrate and gate surfaces, wherein dielectric undercut during this clean process is

prevented by the provision of said nitride plug layer encapsulating and sealing said remaining dielectric layer under each said spacer element;

[c2] The method as claimed in Claim 1, further comprising the steps of: 2. The method as claimed in Claim 1, wherein after step g) the steps of:
(h) forming a respective silicide contact in exposed regions of said semiconductor substrate for contact with a respective source and drain region formed in said CMOS device; and,
i) depositing a contact etch-stop layer which, due to the nitride plug layer formed in step (f), does not come into contact with a gate oxide at an edge of the patterned gate region.

[c3] The method as claimed in Claim 1, wherein step (a) comprises deposition, lithography and etching steps.

[c4] The method as claimed in Claim 3, wherein said spacer is formed sequentially by depositing a conformal nitride layer and anisotropically etching said nitride layer to form each said spacer element at each gate sidewall overlying said dielectric layer.

[c5] The method as claimed in Claim 1, wherein step (d) of removing said dielectric layer, includes implementing a

dry etch process with selectivity such that an edge of said portion of said dielectric layer underlying each said spacer is aligned with a vertical edge of said nitride spacer element.

[c6] The method as claimed in Claim 5, wherein said dry etch process includes a reactive ion etching (RIE) process.

[c7] The method as claimed in Claim 5, wherein said dry etch process includes chemical downstream etching (CDE).

[c8] The method as claimed in Claim 1, wherein step (d) of removing said dielectric layer, includes implementing a wet etch process, said wet etch process being selective and isotropic such that said dielectric layer underlying each said spacer is pulled back out of alignment with a vertical edge of the spacer element.

[c9] The method as claimed in Claim 1, wherein step (f) of creating said nitride plug layer includes implementing a dry etch process that selectively removes nitride.

[c10] The method as claimed in Claim 1, wherein step (f) of creating said nitride plug layer includes implementing a wet etch process that selectively removes nitride.

[c11] A complementary metal oxide semiconductor (CMOS) structure comprising:

a gate region formed on a surface of a semiconductor substrate, said gate including an dielectric layer formed on exposed vertical sidewalls thereof;
a vertical nitride spacer formed on each said vertical sidewall of said gate stack overlying said dielectric layer, whereby a portion of said dielectric layer underlies said vertical nitride spacer and above a substrate surface;
a nitride plug formed over said gate stack, vertical nitride spacer and underlying dielectric layer portion, said nitride plug encapsulating and sealing said underlying dielectric layer;
and,
silicide contacts formed on other portions of said semiconductor substrate adjacent said patterned gate region, for contact with drain and source regions formed in said semiconductor substrate.

[c12] The complementary metal oxide semiconductor (CMOS) structure as claimed in Claim 11, wherein an edge of said portion of said dielectric layer underlying said vertical nitride spacer is aligned with a vertical edge of said vertical nitride spacer element.

[c13] The complementary metal oxide semiconductor (CMOS) structure as claimed in Claim 11, wherein an edge of said portion of said dielectric layer underlying said vertical nitride spacer is pulled back out of alignment with a

vertical edge of said vertical nitride spacer element.

[c14] The complementary metal oxide semiconductor (CMOS) structure as claimed in
Claim 11, wherein said semiconductor substrate is comprised of Si, Ge, SiGe, GaAs, InAs, InP, Si/Si, Si/SiGe, or silicon-on-insulators.

[c15] The complementary metal oxide semiconductor (CMOS) structure as claimed in
Claim 14, wherein said semiconductor substrate is comprised of Si or silicon-on-insulator.

[c16] The CMOS structure of Claim 11, wherein said patterned gate region includes at least a gate dielectric and a gate conductor material.

[c17] The CMOS structure of Claim 16, wherein said gate dielectric is comprised of an oxide, a nitride, an oxynitride, or combinations and multilayers thereof.

[c18] The CMOS structure of Claim 16, wherein said gate dielectric is an oxide selected from the group consisting of SiO_2, ZrO_2, Ta_2O_5, HfO_2 and Al_2O_3.

[c19] The CMOS structure of Claim 16, wherein said gate material is comprised of polysilicon, amorphous silicon, elemental metals that are conductive, alloys of elemental

metals that are conductive, silicides or nitrides of elemental metals that are conductive or any combination thereof.

[c20] The CMOS structure of Claim 19, wherein said gate material is comprised of polysilicon or amorphous silicon.